Notice of Allowability	Application No.	Applicant(s)	
	10/675,674	BELLUOMINI ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *04/03/07*.

2. ☒ The allowed claim(s) is/are *1-3, 5-7, 9, 23-24 now renumbered as 1-9*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

REASONS FOR ALLOWANCE

1. Claims 1-3, 5-7, 9, and 23-24 are allowed.

2. Claims 4, 8, and 10-22 are cancelled.

3. The following is an examiner's statement of reasons for allowance:

The prior art of records fails to disclose or render an obviousness of a fused Booth encoder multiplexer logic cell comprising:

operand bit inputs include a plurality of multiplicand bit inputs and a plurality of multiplier bit inputs, and a given one of said transistor stacks includes: a first logic transistor having a gate controlled by one of said multiplicand bit inputs; a second logic transistor having a gate controlled by a first one of said multiplier bit inputs; a third logic transistor having a gate controlled by a second one of said multiplier bit inputs; and a fourth logic transistor having a gate controlled by a third one of said multiplier bit inputs along with other limitations as cited in an independent claim 1;

a latch includes a first P-MOS transistor having a drain connected to said dynamic node, a source connected to said voltage source, and a gate; a second P-MOS transistor having a gate connected to said dynamic node, a source connected to said voltage source, and a drain connected to said gate of said first P-MOS transistor and said output node; and an N-MOS transistor having a gate connected

to said dynamic node, a source connected to said drain of said second P-MOS transistor, said gate of said first P-MOS transistor and said output node, and a drain connected to electrical ground along with other limitations as cited in an independent claim 23; and

a latch includes a first P-MOS transistor having a gate connected to said dynamic node, a source connected to said voltage source, and a drain; a second P-MOS transistor having a gate, a source connected to said voltage source, and a drain connected to said drain of said first P-MOS transistor; a first N-MOS transistor having a gate connected to said dynamic node, a source connected to said drains of said first and second P-MOS transistors, and a drain; a second N-MOS transistor having a gate connected to said clock input, a source connected to said drain of said first N-MOS transistor, and a drain connected to electrical ground; a third N-MOS transistor having a gate, a source connected to said drain of said first N-MOS transistor, and a drain connected to electrical ground; and an inverter having an input connected to said drains of said first and second P-MOS transistors, and an output connected to said gates of said first P-MOS transistor and said third N-MOS transistor, said inverter output being further connected to said output node to produce an inverted value along with other limitations as cited in an independent claim 24.

The closest found prior arts are the admitted prior art and Houston (U.S. 5,208,489). The admitted prior art in view of Houston disclose a fused Booth encoder multiplexer logic cell comprising a plurality of logic transistors with controlled

respectively by the inputs. However, the admitted prior art in view of Houston fail to disclose the detail structure at the transistor level as seen above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on 7:00AM to 5:00PM M-Th.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C Do
Examiner
Art Unit 2193

May 10, 2007